REMARKS

Claim 1 and 5 have been amended. Thus, Claims 1-8 are pending in the present application. Applicant respectfully requests to enter the above amendment.

Claim rejection under 35 USC §102:

Claims 1, 2, 4-6, and 8 have been rejected under 35 U.S.C. 102(b), as being anticipated by Bartlow (US 5,023,189).

The Examiner states that Bartlow discloses all the limitations of independent claims 1 and 5 and dependent claims 2, 4, 6, and 8. Applicant has amended independent claims 1 and 5 to overcome this rejection. The present invention provides for a simple, accurate and highly efficient way of manufacturing a power transistor circuit. To this end, a die is placed on a substrate carrying at least one input matching element and input signal lead. At this time no connections are established between these elements. However, in the next step, a test network is used to simulate the connections and measure characteristics of the power transistor circuit. The test network comprises connectors with known inductances to establish the respective connections during the measurement. Fig. 6 of the present specification shows an example how a test network is placed on a unwired transistor circuit for testing purposes. Once the measurement has been conducted, the respective necessary inductances for each connection is determined and wiring of the different elements is performed with wires having the respectively determined inductances.

Bartlow on the contrary uses a different approach which is more costly and cumbersome. According to Bartlow, (1) a die is placed on a substrate and (2) all elements are wired using the regular bonding technique. See Bartlow, col. 3, lns. 46-55. Then, (3) the circuit is test under DC and/or RF conditions and a thermal scan is performed. See Bartlow, col. 3, lns. 55-59. Then, (4) all wires are removed and a different set of wires is used. See Bartlow, col. 3, lns. 59-62. Then, the steps (2) – (4) are repeated until the desired result is obtained. See Bartlow, col. 3, lns. 62-65. Because Bartlow never knows what inductances are used for the respective wires, Bartlow teaches a trial and error method which requires multiple iterations to generate the required result. In addition, each iteration requires the actual bonding of the respective elements. This is an

additional costly process because if the iteration step was not successful, removal of the wires is required.

The present invention is, therefore, much more efficient because according to the present invention the inductance parameter for each wire can be determined. This is possible because during testing the inductance of each connection which is established by the test network is known.

Claims 2, 4, 6 and 8 are dependent claims which include all limitations of at least the respective independent claims 1 or 5. Therefore, these claims are allowable at least to the extent of the respective independent claim 1 or 5.

Claim rejection under 35 USC §103:

Claims 3 and 7 have been rejected under 35 U.S.C. 102(b), as being unpatentable over Bartlow (US 5,023,189) in view of Mazuno et al. (JP406006150A) and Shimizu et al. (US 6,331,804).

Claims 3 and 7 are dependent claims which include all limitations of at least the respective independent claims 1 or 5. Therefore, these claims are allowable at least to the extent of the respective independent claim 1 or 5.

CONCLUSION

As hereby amended, claims 1-8 are pending in the application. The application as defined in the pending claims is patentable under 35 U.S.C. 102 in view of Bartlow and under 35 U.S.C. 103 in further view of Mazuno and Shimizu. Therefore, applicants respectfully request withdrawal of the rejection and allowance of all pending claims.

Applicants do not believe that any other fees are due at this time; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to this document, the Commissioner is authorized to deduct the fees from Deposit Account No. 02-0383, *(formerly Baker & Botts, L.L.P.)* Order Number 071308.0168.

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